IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

THE TRUSTEES OF PURDUE UNIVERSITY, Plaintiff, v. STMICROELECTRONICS N.V., STMICROELECTRONICS INTERNATIONAL N.V., and STMICROELECTRONICS, INC, Defendants.	CIVIL ACTION NO. 6:21-CV-00727-ADA JURY TRIAL DEMANDED

DECLARATION OF ISHWARA BHAT, PH.D. IN SUPPORT OF PLAINTIFF'S SURREPLY CLAIM CONSTRUCTION BRIEF

I, Ishwara Bhat, hereby declare as follows:

1. The following opinions supplement those in my prior declaration in this case, signed on March 14, 2022, in response to Defendants' Reply Brief concerning the claim construction for U.S. Patent Nos. 7,498,633 ("'633 Patent") and 8,035,112 ("'112 Patent") (together, the "Asserted Patents") and the Rebuttal Declaration of Defendants' expert, Dr. Subramanian ("Subramanian Rebuttal Decl.").

2. While this Declaration addresses several arguments made in Dr. Subramanian's Rebuttal Declaration, I note that Dr. Subramanian considers draft claims that were discarded during the prosecution of the Asserted Patents, as well as claims that are not asserted in the present litigation, such as claims 12 and 15 of the '633 Patent. I consider those items to be outside the scope of the claim construction issues that I opine on.

3. All of the opinions stated in this Declaration are based on my personal knowledge and professional judgment. If called as a witness, I am prepared to testify competently about them.

4. I reserve the right to supplement, clarify, modify and/or change my testimony as

additional facts, questions, or issues come to my attention.

5. This Declaration must not be construed as expressing opinions on matters of law, which are for the Court to determine, although it necessarily reflects an understanding thereof.

I. DIFFERENCES IN THE DESIGN OF SILICON CARBIDE AND SILICON DEVICES

6. A true POSITA would know that the parameters I identified in my prior declaration, such as on-resistance and blocking voltage, drift region resistance, maximum electric field in the oxide under the gate, maximum JFET width, and channel resistance versus drift-region resistance must *always* be considered when designing silicon carbide ("SiC") MOSFETs. They are the relevant aspects of physics governing such semiconductor devices. A POSITA would recognize that the width of the JFET region is critical to the reliability of SiC power MOSFETs, a consideration absent from their silicon counterparts. A proper SiC power MOSFET design must successfully address the risk created by the high electric field in the oxide between the gate and the JFET region and the challenges that JFET-region width creates to reach a high blocking voltage. Thus, designing the right JFET-region width plays an important part when optimizing a high-voltage SiC MOSFET's on-resistance. This is not the case for silicon devices where the oxide on the JFET region is not exposed to such intense electric fields.

7. A true POSITA would also understand that once the issue of JFET-region width is addressed, the other resistive elements that I referred to, such as the source-contact resistance, gain importance in ways that are specific to SiC devices and differ significantly from silicon devices. I, therefore, disagree with Dr. Subramanian's statement that these resistive elements are parameters that are not specified in the '633 Patent. Subramanian Rebuttal Decl., ¶ 7. For instance, claim 9 addresses the resistivity of the source contacts by reciting a specific design for the source and base electrode and contacts. This design is explicitly described in the '633 Patent, which explains how

the source-contact resistance is decreased by the design recited in claim 9. *See* '633 Patent at 7:52-67, 8:1-28.

8. The '633 Patent also states that eventually "the specific on resistance contribution of a JFET region of a MOSFET device is reduced to a point where at the source resistance of the device becomes one of the dominating contributions to the specific on-resistance of the device". *Id.* at 7:22-26. A true POSITA would know that this statement, in addition to (1) the elements recited in claim 9 and (2) the high-voltage DMOSFET exemplary embodiments listed in the specification (e.g., a 1000-volt DMOSFET) show that they are directed solely to SiC DMOSFETs and cannot apply to silicon DMOSFETs. *Id.* at 4:59-60. This is because the drift-region resistance makes an overwhelming contribution to the specific on-resistance of a silicon DMOSFET, rendering the '633 Patent's focus on other resistive elements inefficient. Furthermore, DMOSFET designs, such as those of the '633 Patent, do not function well in silicon for blocking voltages higher than a few hundred volts due to excessive on-resistance, which is why they give way to different silicon devices, such as Superjunction MOSFETs and IGBTs.

9. Dr. Subramanian opines that the '633 Patent was meant to cover silicon devices as well as SiC devices, but I believe that a true POSITA would not view any of these statements as pertinent to the claims at issue. Subramanian Rebuttal Decl. ¶¶ 8-10. For example, while the specification states that the "semiconductor substrate ***may be*** formed from a silicon carbide material," claim 9—the only claim at issue—explicitly requires a "silicon-carbide substrate" and does not suggest any alternative materials.

II. DISPUTED CLAIM TERMS OF THE '112 PATENT

A. "a second, thicker oxide layer over said top surface and sidewall of each of said first gate"/ "a gate oxide layer thicker than said substrate surface oxidation layer, over said tops and sides of each of said gates"

10. In his declaration, Dr. Subramanian explains the traditional way of making a source contact using conformally deposited oxide layer discussed in the Dr. Baliga manual. Subramanian Rebuttal Decl., ¶¶ 11-15. However, the claims of the '112 Patent do not recite or require deposition techniques such as the one set out in the Baliga reference, which is only one of many ways of making the source contact.

11. Instead, the '112 Patent describes an improved design that creates an insulating layer on the polysilicon gate that is thicker than that on other areas such, as the SiC on the MOSFET surface. This design is well-suited for SiC because it helps reduce the resistance of the source contact, which is a significant contributor to specific on-resistance and could make use of growth or deposition processes. While many deposition processes coat the surface of the layer conformally without regard to the nature of the substrate, this only holds true when the substrate temperature is low or when the deposition chemistry does not involve any reaction with the surfaces. The deposition rate can be made surface dependent by increasing the temperature or facilitating a chemical reaction. This deposition process is called "selective" deposition. It can be used in SiC to form a thicker oxide or insulating layer surrounding a polysilicon gate than on a SiC substrate surface, as the gate will react more than the SiC. It is an alternative to growing oxide thicker on the gate than on a SiC substrate surface. Thus, a POSITA would not read the specification to limit the invention to SiC MOSFETs, where oxide layers are grown.

III. DISPUTED CLAIM TERMS OF THE '633 PATENT

A. Whether the preamble of Claim 9 is limiting

12. Dr. Subramanian opines that once one sets aside the recitation of a SiC DMOSFET

in the preamble of claim 9, "the specification suggests that other types of devices are within the scope" of the claim. Subramanian Rebuttal Decl., ¶ 16. But the cited passage of the specification refers only to "other types of MOSFET devices," and thus, does not envision devices other than MOSFETs. *See* '633 Patent at 4:4-12. As I explained in my prior declaration, SiC and double implantation are written into the limitations in the body of claim 9 itself, namely in the requirements of "a silicon-carbide substrate" and "a plurality of [first/second] base contact regions defined in the [first/second] source region." It is, therefore, incorrect to say that a POSITA would understand that another type of MOSFET, or another kind of device, would be covered by the claim upon reading the body of claim 9 in combination with the '633 Patent specification.

B. "less than about three micrometers"

13. As I stated in my prior declaration, a variation of ±10% during manufacturing is expected when numerical values are used for the JFET regions of SiC DMOSFETs and this is exactly how a POSITA would understand the word "about" in the limitation of a JFET width "less than about three micrometers" with reasonable certainty.

14. In response, Dr. Subramanian opines that the *Ryu* article, Exhibit C to my prior declaration, features a design specification with a "66.7% increase" from the desired 3-micrometer JFET width and that this is inconsistent with my opinion "that a dimension such as the 3 micrometer JFET gap would be understood to be +/- 10% to account for these very same manufacturing issues." Subramanian Rebuttal Decl., ¶ 20. But Dr. Subramanian makes a fundamental mistake that a POSITA would know to avoid, i.e., conflating two separate issues. The first issue is that a ±10% variation is the expected value for tolerances in the lithography and etching in a typical manufacturing facility. *See, e.g.*, Ex. A, Wolf and Tauber, *Silicon Processing for the VLSI Era*, Vol. 1, Lattice Press (2000)", at p. 533 (referencing this 10% tolerance for polysilicon lithography and etching, which applies to polysilicon used on both SiC and silicon

wafers). In practice, the variation depends on many factors, including the equipment set and the competence of the manufacturing facility. For example, a research lab or a medium-sized company (such as the ones where the authors of the reference worked at the time) may have a much higher variation than a state-of-the-art facility in a leading semiconductor fab.

15. The second issue is that manufacturing facilities may experience difficulties with achieving precise doping values and controlling dopants' encroachment into the JFET region due to transverse or lateral straggle in the ion-implantation process. This may lead researchers to use masks widths that are much larger than the desired JFET width. In the *Ryu* article I referenced in my prior declaration, the starting value of the polysilicon mask width is set at 5 micrometers (thus 66.7% larger than the intended JFET region), so that the JFET width in the finished device will be close to 3 micrometers. *See* Dkt. 70-4 at H4.5.2 ("JFET gap of 5 um was used to account for implant straggles and other process biases."). A true POSITA would understand that the finished device's JFET width will be equal to the mask width minus twice the lateral straggle of the ion-implantation process, therefore a 3-micrometer mask would result in a much narrower JFET region. No true POSITA would take the mask dimension as an indication that the JFET width could vary up to the size of the mask.

16. Dr. Subramanian further opines that "nothing in the patent or prosecution history to indicate what objective is intended with respect to the JFET width limitation." Subramanian Rebuttal Decl., ¶ 17. This is also incorrect. The '633 Patent specification clearly states that the JFET width is optimized according to two objectives: (1) decreasing on-resistance and (2) reducing the electric field in the oxide above the JFET region. '633 Patent at 6:21-27, 6:45-50. In addition to these stated objectives, a true POSITA would know that there are mandatory objectives for SiC JFET-region design, such as ensuring good forward current conduction and withstanding reverse

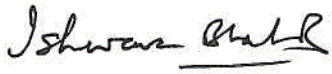
blocking voltage.

17. Dr. Subramanian's assertions regarding the specific voltages, thicknesses, or doping concentrations employed in the *Ryu* article or even with respect to claim 9 are misplaced because the design of SiC power devices differs from that of silicon devices. Subramanian Rebuttal Decl., ¶¶ 19-20. In the design of a SiC DMOSFET, the goal is always to craft a device with the lowest possible on-resistance for the rated blocking voltage. Whatever the blocking voltage, the maximum electric field at the boundary of the base region and the drift region is designed to be close to the critical electric field for silicon carbide (which is 7-10 times higher than in silicon). If this high electric field reaches the surface of the JFET region, there will be catastrophic failure of the oxide since the electric field in the silicon dioxide below the gates is about 2.5 times higher than that of the SiC of the JFET region. Thus, the JFET width has to be carefully designed to keep the electric field on the surface of the SiC below a value so the field in the oxide does not exceed the maximum sustainable value of 4×10^6 V/cm, a value considered to be the long-term reliability limit. This is not the case for silicon as the maximum electric field in silicon is low enough such that the electric field in the oxide will never exceed $3x10^6$V/cm. Since these electric field values are generally fixed for a SiC device irrespective of the blocking voltage, the JFET width does not change significantly to a first approximation. That is why Dr. Subramanian's critique that optimal values for JFET regions should be linked to specific device parameters (*id*., ¶¶ 21-23) might be sensible for silicon devices but is completely inapposite in SiC and, in particular, to the invention of claim 9 of the '633 Patent.

18. Dr. Subramanian does not dispute that the lower bound for JFET width is limited by manufacturing process technology but contends the '633 Patent specification offers no support and the inventors' article cited in my prior declaration shows that $R_{on,sp}$ increases dramatically

below a JFET width of one micrometer, which would negatively affect device performance. Subramanian Rebuttal Decl., ¶ 22. Regardless, a POSITA would know that the JFET width cannot be arbitrarily reduced to an infinitesimal dimension, such as 0.001 micrometer or 0.0001 micrometers (0.0001 micrometers is less than half the size of a single silicon atom, which measures 0.00024 micrometers), or to zero (in which case the device could not be a DMOSFET at all).

19. A true POSITA would also be well aware that semiconductor physics predict the rise in specific on-resistance for JFET widths far below 1 micrometer. The current has to go from the source through the channel and through the JFET region and then down to the drain. The effective JFET region width is the metallurgical JFET width, as described in the '633 Patent minus twice the depletion layer width in the JFET region of the p-base-n-drift region junction. A typical SiC depletion layer width for zero bias based on the doping can be calculated from elementary p-n junction theory to be about 0.3 micrometers. As such, the JFET width at the lower bound is 0.6 micrometers plus the required JFET width for current flow with the needed resistance plus any limits based on the process manufacturing technology. As a result, JFET width around 1 micrometer (as mentioned in the '633 Patent) present a realistic value based on the $R_{ON,SP}$ design and certainly cannot go below 0.6 micrometers. *See*, *e.g.*, Dkt. 70-3 at ST-PURDUE_00003135.



04/11/2022

Date

Ishwara Bhat, Ph.D.